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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/039,060 | 01/02/2002 | Sujat Jamil | 42390P12483 | 9109 |

8791 7590 11/10/2005

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| EXAMINER | |
|---|---|
| LANE, JOHN A | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2185 | |

DATE MAILED: 11/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/039,060 | JAMIL ET AL. | |
| | Examiner | Art Unit | |
| | Jack A. Lane | 2185 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *09/30/2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. This Office action is responsive to the amendment filed 09/30/2005. Claims 1-26 are presented for examination. Any objections or rejections made in the previous office action not specifically repeated below are withdrawn or have been overcome by applicant's response.

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 09/30/2005 has been entered.

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. section 103 (a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 C.F.R. 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 1-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli et al. (6,292,872) in view of the standard practice of integrating circuits, as further evidenced by Sherburne (2002/0184546).

Arimilli discloses a plurality of processor units (10a-10n), a plurality of cache units (12a-12n), one of the cache units provided for each one of the processor units, a cache coherent bus 16 coupled to the processor units, the bus configured to provide cache coherent snooping commands from the processor units themselves (col. 9, lines 39-45) to ensure cache coherency between the cache units for the processor units and the embedded RAM unit (e.g., col. 2, lines 1-5). Arimilli does not expressly mention a particular embodiment of an integrated circuit, however the Examiner takes Official Notice that it is manifestly obvious to integrate multi-processing devices for the well-known and well-noted advantages of portability, power consumption, and so forth. This is further evidenced by Sherburne. Sherburne discloses the well-known practice of using highly integrated devices to obtain the advantages of decreased size and weight (e.g., paragraph (0002)).

It would be obvious to combine Arimilli with the well-known practice of integration because the practice is standard and the advantages for doing so are well established in areas such as those evidenced by Sherburne, which included multiprocessing systems with cache and embedded memory. Therefore it would be obvious to one of ordinary skill in the art to combine Arimilli with the standard practice of integration.

The examiner believes all dependent claim features not specifically discussed above are expressly or inherently taught by Arimilli or Sherburne. The remaining dependent claim features, while part of the invention, do not appear essential to the main invention found in the

independent claims. Thus, a detailed discussion of the well known claim feature(s) is not warranted at this time. Support for this line of reasoning is derived from 37 C.F.R. 1.105. 37 C.F.R. 1.105 permitting "stipulations as to facts" or "whether a dependent claim element is known in the prior art based on the examiner having a reasonable basis for believing so."

In the Remarks filed 09/30/2005, Applicant argues the following:

> The Final Office Action performs a complex analysis of the Arimilli reference in order to conclude ....Nevertheless, applicants submit that Arimilli, at best, discloses transferring data from a first dedicated processor cache to a second processor to be processed at the second processor upon cache misses at a second dedicated processor cache...Applicant's maintain that nowhere...suggestion of transferring cache lines from one dedicated processor cache to another dedicated processor cache.

Applicant presented a similar argument in the Remarks filed 06/02/2005:

> As discussed above, neither Arimilli nor Sherburne disclose or suggest transferring a cache line from a first dedicated processor cache and to transfer the first cache line to a second dedicated processor cache. Arimilli discloses an architecture having dedicated processor caches. However, there is no disclosure of control logic that transfers cache lines between the dedicated processor caches.

In response, Applicant should reconsider the following presented in the final Office action mailed 06/28/2005:

As found in Arimilli (6,292,872) col. 6, lines 11-18 and 35-41:

> If however, the read request misses in both L1 cache 12a and L2 cache 14a, cache controller 36 of L2 cache 14a presents the read request as a transaction on interconnect 16, which is **snooped**...In response to **snooping** the read request..., cache controller 36...determines if the requested data is resident in...the associated one of L1 caches 12b-12n.
>
> If the data requested...is stored, for example, in L1 cache 12n..., cache controller 36...signals L1 cache 12n to push the requested data to L2 cache 14n . L2 cache 14n sources the requested data on interconnect 16 (*to the requesting processor*).

Given the above disclosure it is clear that the cache controller 36 of Arimilli corresponds to the claimed control logic and can transfer data (i.e. cache lines) between dedicated processor L1 caches (12a and 12b-n).

**Any response to this action should be mailed to:**

Under Secretary of Commerce for Intellectual Property and Director of the United States Patent and Trademark Office
PO Box 1450
Alexandria, VA 22313-1450

**or faxed to:**

(571) 273-8300, (for Official communications intended for entry)

**Or:**

(571) 273-4208, (for Non-Official or draft communications, please label "Non-Official" or "DRAFT")

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jack A. Lane whose telephone number is 571 272-4208. The examiner can normally be reached on Mon-Fri from 7:30AM-6:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 571 272-4210.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 571 272-2100